Electrical properties of MOS circuit

Electrical properties of MOS circuit :

- Parameters of MOS transistors, pass transistors,
- N MOS inverter,
- Pull-up to pull down ratio for an N MOS inverter,
- C MOS inverters,
- MOS transistor circuit model,
- Latch up on C MOS circuits.

Parameter of MOS

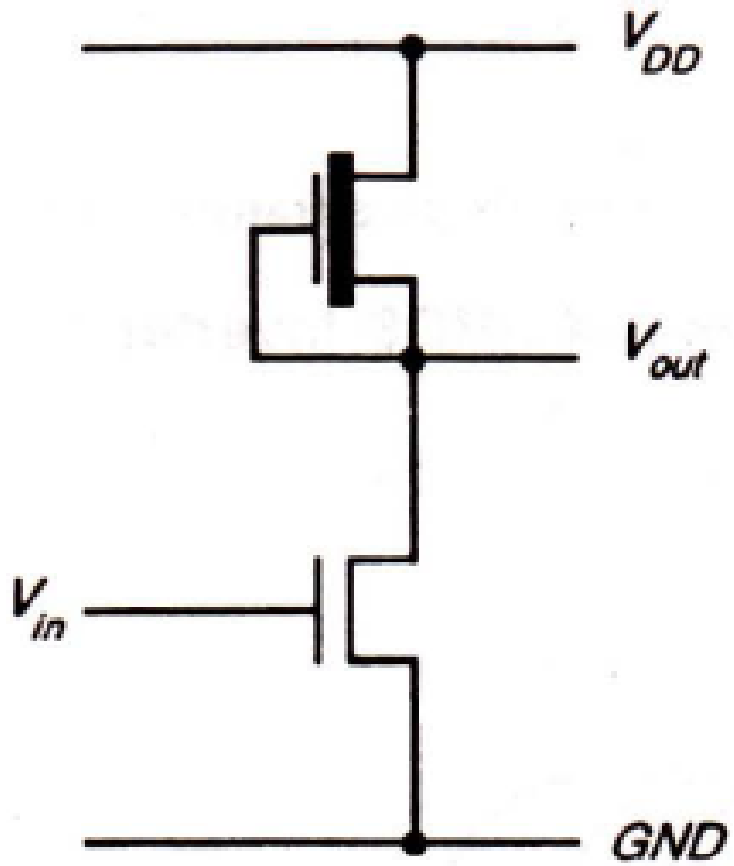
- Transconductance expresses the relationship between output current *Ids and the input voltage Vgs and is defined as*

$$g_m = \frac{\delta I_{ds}}{\delta V_{gs}} \Big| V_{ds} = \text{constant}$$

- The output conductance *gds can be expressed by*

$$g_{ds} = \frac{\delta I_{ds}}{\delta V_{gs}} = \lambda . I_{ds} \; \alpha \left(\frac{1}{L} \right)^2$$

NMOS Inverter

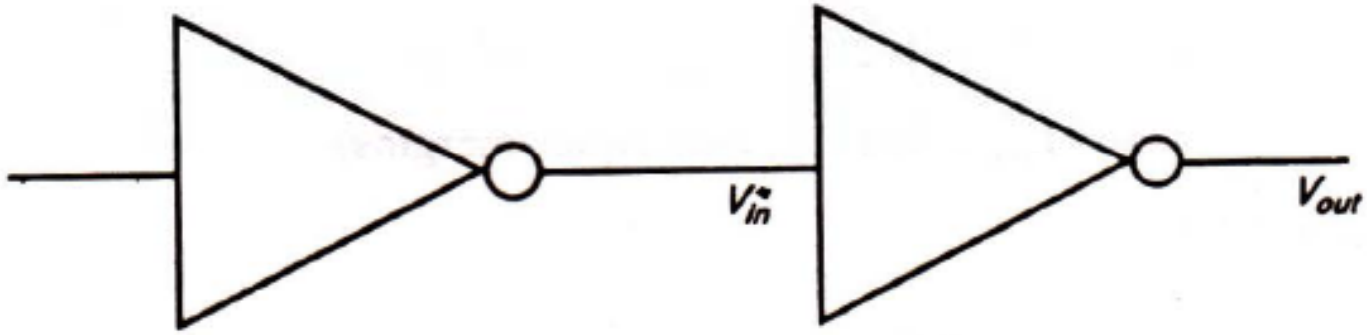


With no current drawn from the output, the currents *Ids for both transistors must be*
equal.

- For the depletion mode transistor, the gate is connected to the source so it is always
on and only the characteristic curve *Vgs = 0 is relevant.*
- In this configuration the depletion mode device is called the pull-up (p.u.) and the
enhancement mode device the pull-down (p.d.) transistor.

Pull-up to pull down ratio for an N MOS inverter,

$$V_{in} = V_{out} = V_{inv}$$

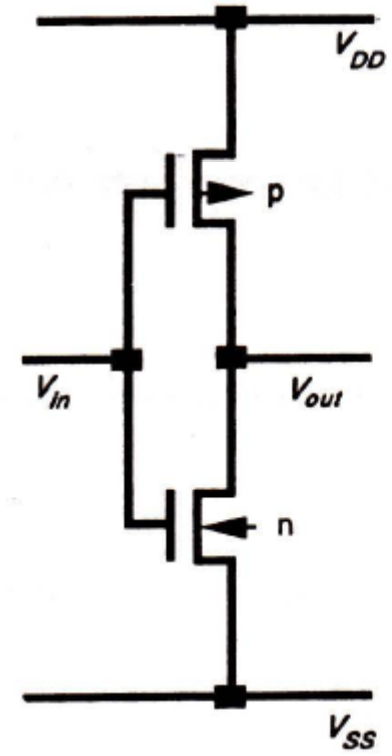


$\sqrt{Z_{p.u.}/Z_{p.d.}} = 2$

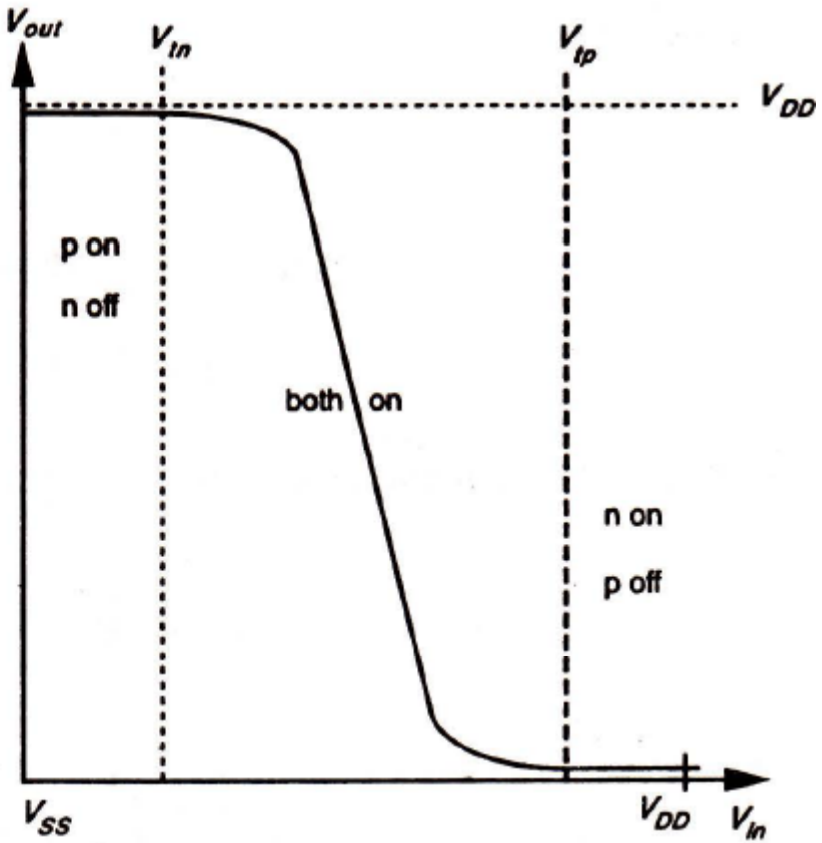
$Z_{p.u.}/Z_{p.d.} = 4/1$

$$V_{inv} = V_t - \frac{V_{td}}{\sqrt{Z_{p.u.}/Z_{p.d.}}}$$

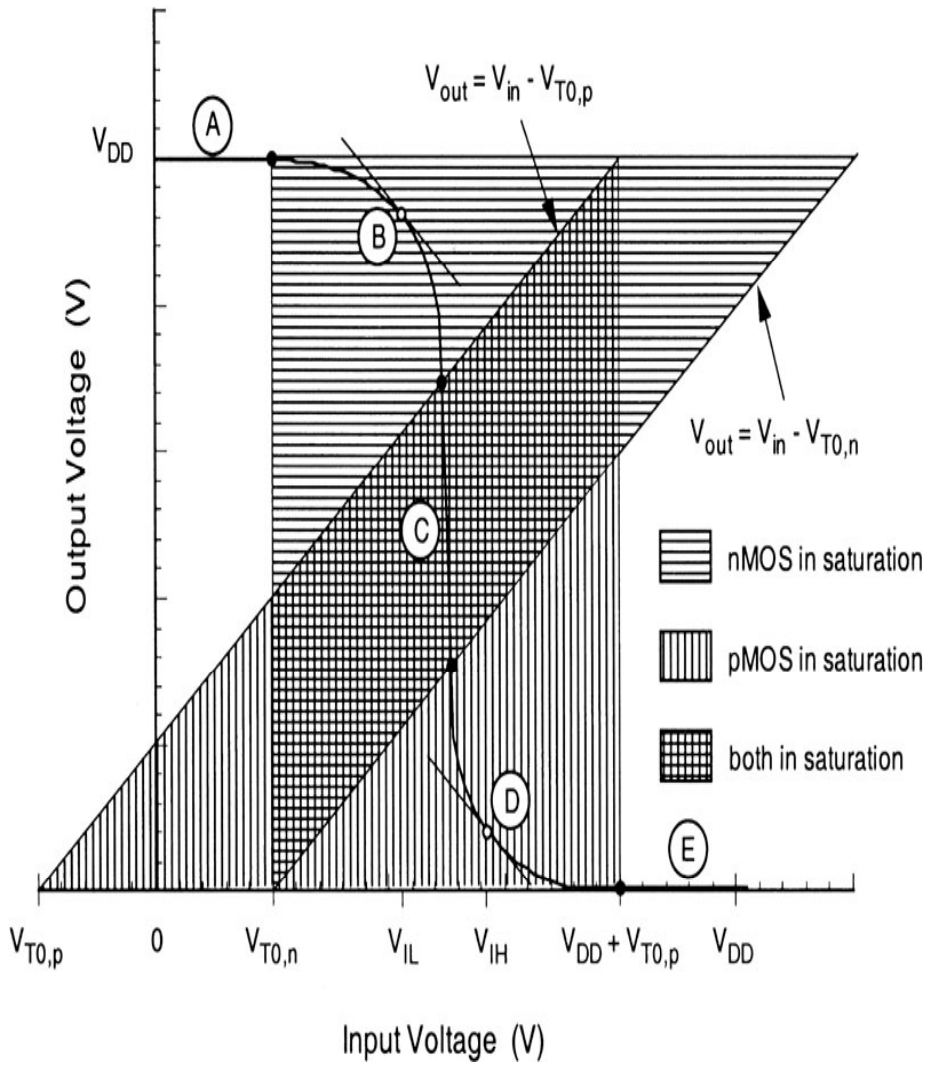
CMOS Inverter



(a) Circuit

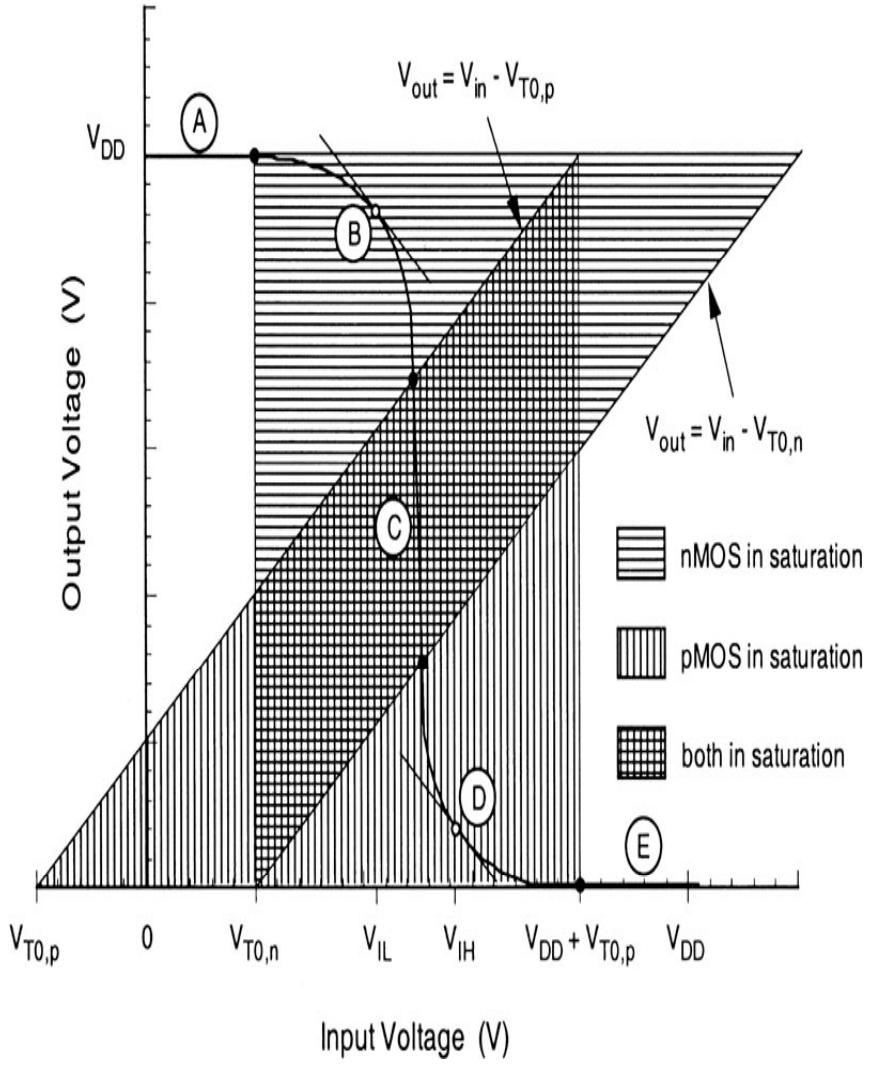


(b) Transfer characteristic



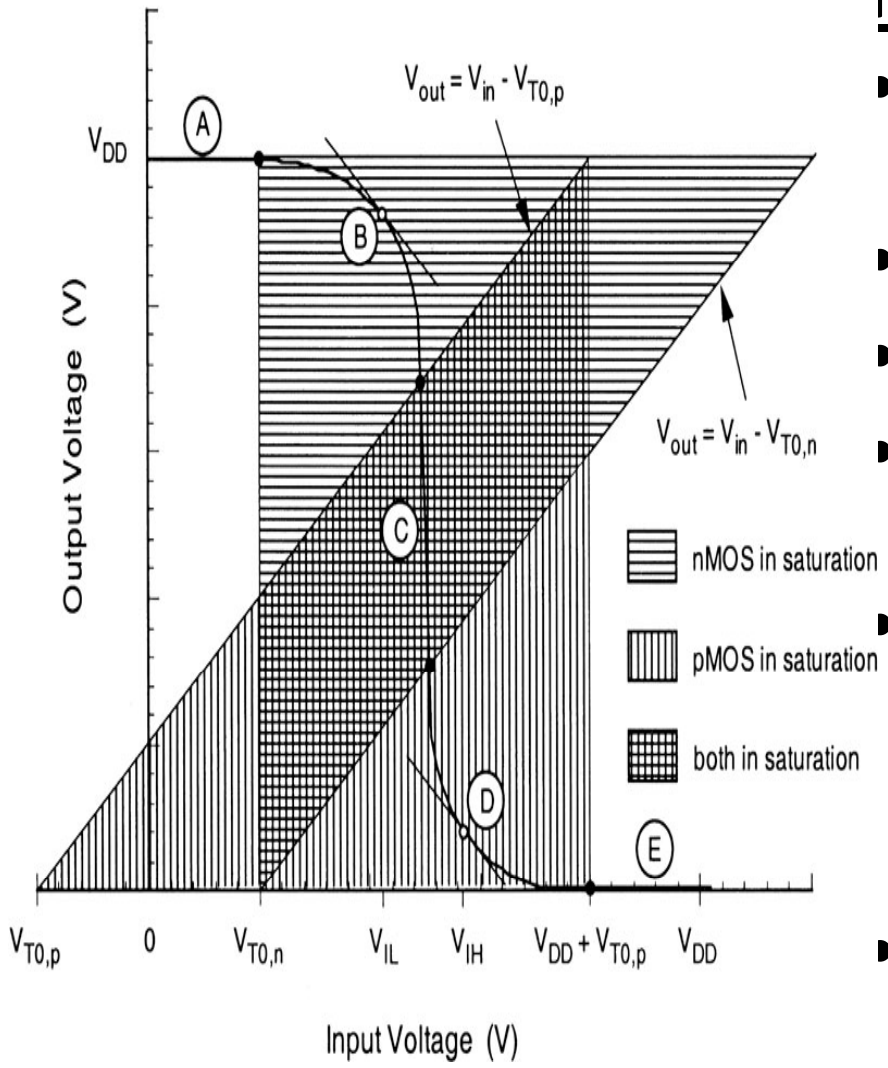
In Region 1:

- V_{in}= 0
  - PM=ON
  - NM=OFF
- No current is flowing through the inverter
- $V_{out} = V_{DD}$ ='1'
- V_{out} is pulled up to V_{DD} through PMOS



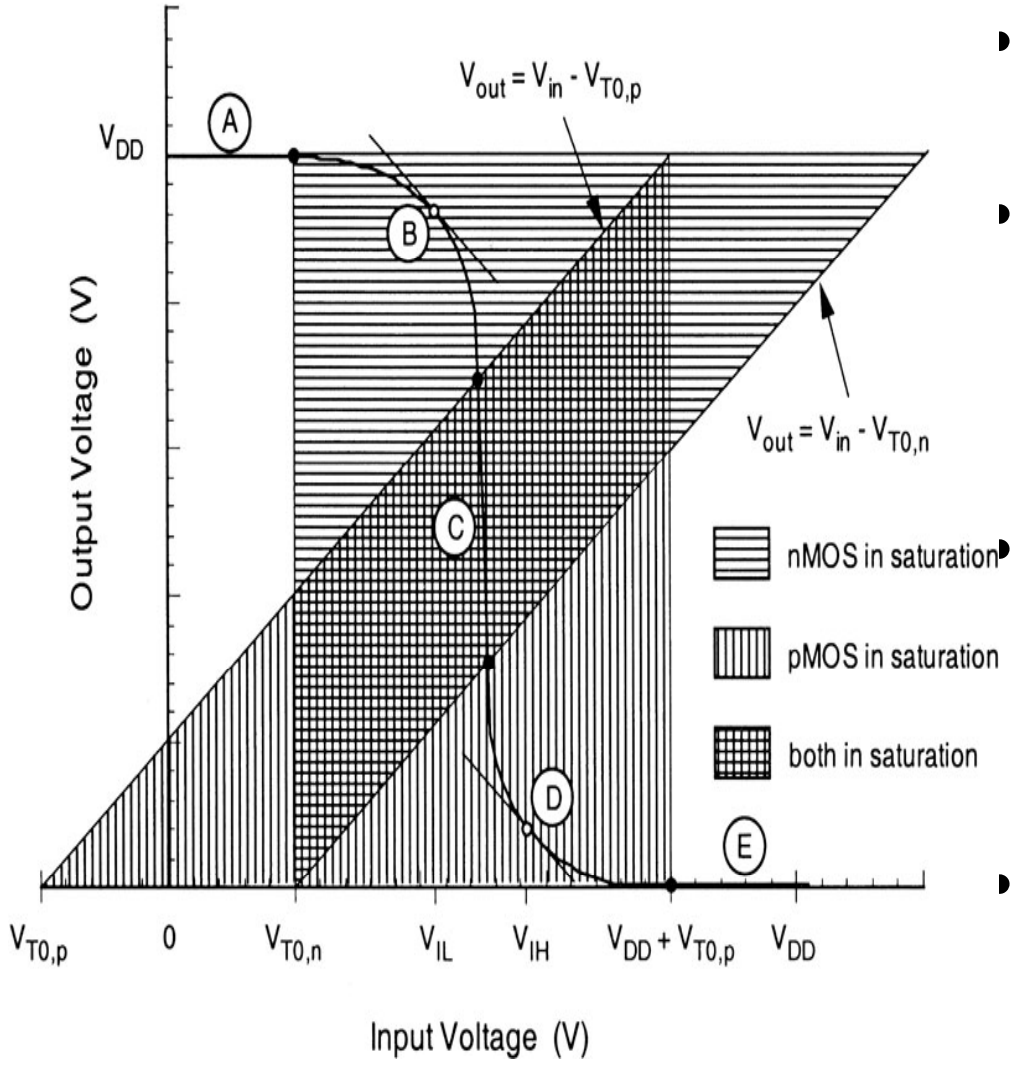
In Region II:

- Increase the input voltage beyond logic 0
- Voltage crosses the threshold voltage $(V_t)_N$ of nMOS transistor
  - $V_{in} > (V_t)_N$
  - NMOS starts conducting and goes to saturation
- Similarly $V_{in} < (V_t)_P$
  - PMOS starts conducting and region of operation is called Linear/ NON Saturated/ Resistive mode
- V_{out} start to decrease & a small amount of current start to flow from V_{DD} to GND



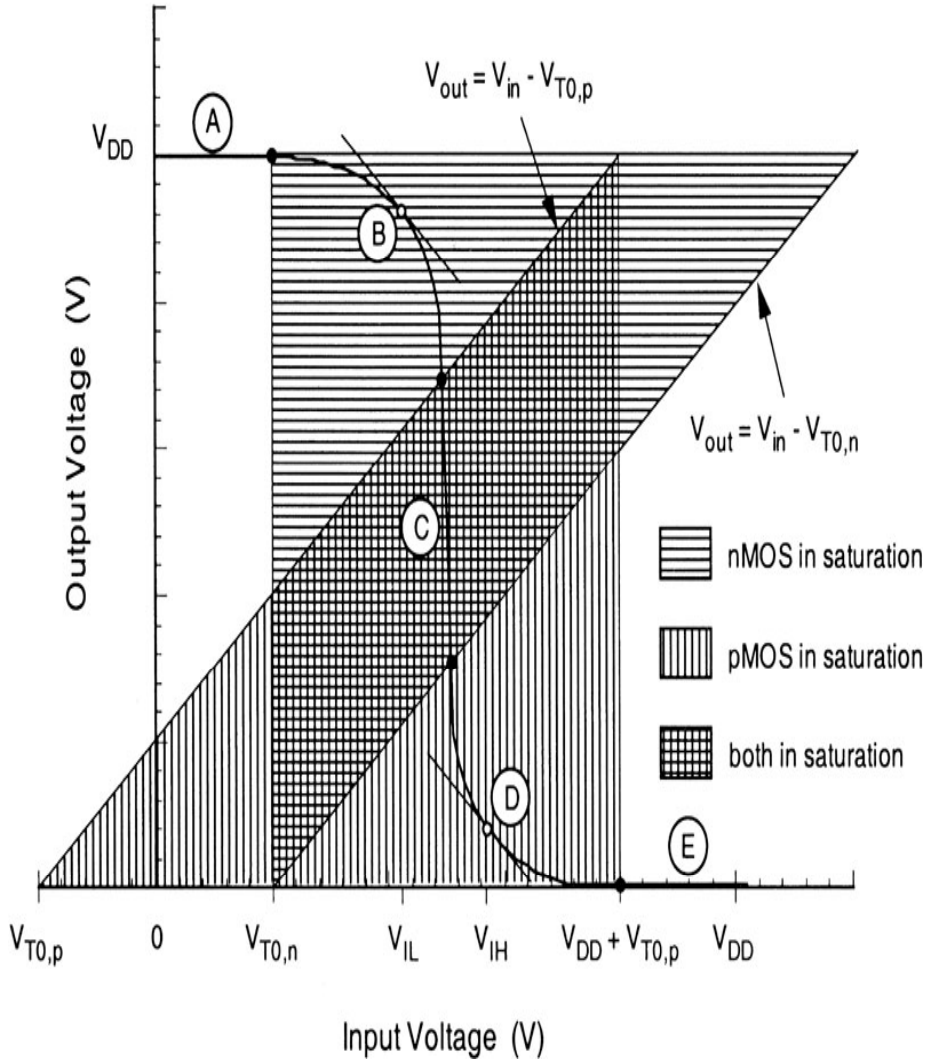
In Region III

- I/p voltage is further increased
- PM goes in saturation
- NM also in saturation
- CMOS exhibits maximum gain
- More energy is consumed; when CMOS inverter switches from one state to other
- Maximum amount of current flows between V_{DD} to GND



In Region IV

- I/p voltage is further increased
- NM remains in conducting mode but it has only a small voltage across it
  - Operate in linear
- Now PM conduct heavily and has large voltage across it
  - Comes to saturation mode
- Again current flowing between V_{DD} and GND decreases



- **<u>In region V</u>**

  When i/p voltage approaches V_{DD}
  - NM- ON
  - PM – OFF

  Again no Current flow through inverter i.e. V_{DD} to GND
  - V_{out} = GND

  V_{out} is pulled down to ground through NMOS transistor i.e. NM
  - V_{out} =0

MOS TRANSISTOR CIRCUIT MODEL

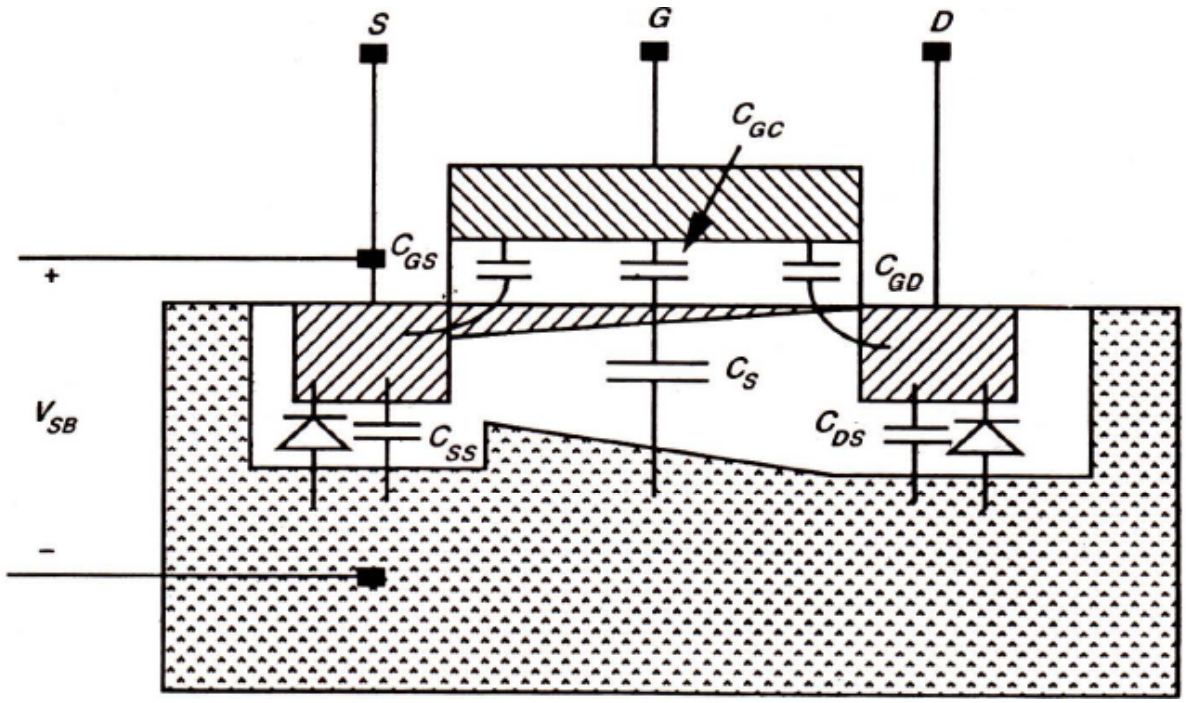


FIGURE 2.16 nMOS transistor model.

es: C_{GC} = gate to channel capacitance
C_{GS} = gate to source capacitance
C_{GD} = gate to drain capacitance
} Small for self-aligning nMOS process

Latch Up for CMOS

- Latch-up may be induced by glitches on the supply rails or by incident radiation.
- The mechanism involved may be understood by referring to Figure which shows the key parasitic components associated with a p-well structure in which an inverter circuit (for example) has been formed.